L3: Entry 17 of 157 File: USPT Jun 10, 2003

DOCUMENT-IDENTIFIER: US 6578102 B1
TITLE: Tracking and control of prefetch data in a PCI bus system

Detailed Description Text (15):
One method for reducing latency is the prefetch operation in which data is read from a data source in anticipation that a requesting data destination will need the data. The data is read from the data source and stored in a prefetch buffer 80, 82 and then is read from the prefetch buffer by the requesting data destination device, such as a channel adapter 14A-D. Thus, in a complex bus system, as discussed in the incorporated '610 application, read transactions of multiple agents, such as channel adapters 14A-D, are allowed to be processed in parallel by allowing prefetched data blocks for different requesting agents to be stored in different parallel prefetch locations which are arranged as parallel FIFO buffers 80, 82. Referring additionally to FIG. 3, each channel adapter 14A-D attached to the remote bridge 18 has a parallel FIFO buffer comprising a section or location of a FIFO buffer 80, 82. In FIG. 3, the sections of FIFO buffers 80 may comprise buffers 91-96, each having the appropriate load/unload circuitry, and be assigned, respectively, to the channel adapters 14A, B, C, D and other agents coupled to the secondary PCI bus 44, such as PCI bus adapters 50, 52, for read operations. As discussed in the incorporated '610 application, other sections of the FIFO buffers may be employed for write operations and for control.